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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/797,621	03/10/2004	Enrico Temporiti Milani	851863.411	4753

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EXAMINER	
LUU, AN T	

ART UNIT	PAPER NUMBER
2816	

DATE MAILED: 04/05/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/797,621	TEMPORITI MILANI ET AL.	
	Examiner	Art Unit	
	An T. Luu	2816	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *15 February 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-9,11,12 and 15-23* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-9,11-12,15-23* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Applicant's Amendment filed on 2-15-06 has been received and entered in the case. Claims 1-9,11-12 and 15-23 are pending. The rejection of claims, presented in the previous Office Action, is maintained.

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claims 1-3, 5 and 8-10 are rejected under 35 U.S.C. 102(b) as being anticipated by the Partovi et al reference (U.S. Patent 5,963,059).

Partovi et al discloses in figure 8 a phase detector comprising a first bistable element 804 clocked by the first signal Fin and having a first output (i.e., output of 808) a second bistable element 802 clocked by the second signal Fref and having a second output signal (i.e., output of 806); means for determining the change of said phase difference signal (i.e., charge pump as shown in fig 1), responsive to said first and second output signals, and a reset circuit (828, 820, 824, 822, 826) having a first and a second inputs respectively connected to said first and second output signals and adapted to determine the resetting of the first and the second bistable elements responsive to the attainment of a respective prescribed state on the part of the first and the second output signals, said first and second inputs of the reset circuit substantially symmetrical to each other from the point of view of a respective input impedance associated with each of them (i.e., 832 and 830 are symmetrically coupled to 828); and a symmetrization element (832 and 830)

coupled to the output terminals of the first and second bistable elements as required by claim 1. It is noted that the symbol of inverter, as shown, represents two transistors coupled in series (i.e., same branch) having gates coupled to a common node.

As to claim 2, inverter 832 and 830 are seen as input impedance symmetrization means.

As to claim 3, fig. 8 discloses a logic circuit 828 with a first logic input and a second logic input, respectively coupled to the first and the second signals and adapted to detect the attainment of the respective prescribed state by the first and the second output signals, and in which said symmetrization means are associated with said first and second logic inputs.

As to claim 5, figure 1 discloses a phase difference detector 102 adapted to detect a phase difference between the reference signal (Fin) and a signal derived from the output signal (Fout), and an oscillator 106 controlled by a phase difference signal (output of 102) generated by the phase difference detector, characterized in that the phase difference detector is realized according to claim 1 (See the rejection of claim 1 as noted above).

As to claim 8, it is inherent that there exists a generator to generate a reference signal.

As to claim 9, it is rejected for reciting a method/step derived from an apparatus of claim 1 which is rejected as noted above.

As to claim 10, the scope of claim is similar to that of claim 1. Therefore, it is rejected for the same reason set forth above.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 1-9, 11-12 and 15-23 are rejected under 35 U.S.C. 103(a) as being unpatentable over the Nilsson reference (U.S. Patent 6,605,935) in view of the Pricer reference (US Patent 5,673,005).

Nilsson disclose in fig 11 a phase detector comprising a first bistable element 1001 clocked by the first signal (fref) and having a first output (source) a second bistable element 1003 clocked by the second signal (Presc) and having a second output signal (sink); means for determining the change of said phase difference signal (charge pump; 1105 and 1107), responsive to said first and second output signals, and a reset circuit 1109 having a first and a second inputs respectively connected to said first and second output signals and adapted to determine the resetting of the first and the second bistable elements responsive to the attainment of a respective prescribed state on the part of the first and the second output signals, said first and second inputs of the reset circuit substantially symmetrical to each other from the point of view of a respective input impedance associated with each of them (i.e., 1113 and 1115 are symmetrically coupled to 1109) and a symmetrization element (1113 and 1115) coupled to the output terminals of the first and second bistable elements as required by claim 1.

Nilsson does not disclose delays 1113 and 115 including two transistors as required by the claim.

Pricer disclose in figure 3 a delay 31 comprising two transistors 34 and 35, coupled in series (i.e., same branch) having gates terminal coupled to an input 32 as required by claim.

It would have been obvious to one skilled in the art at the time the invention was made to realize a delay of Nilsson with the one taught by Pricer since the delay of Pricer would provide a capability of independent from variations of temperature and supply voltage.

As to claim 2, delays 1113 and 1115 are seen as input impedance symmetrization means.

As to claim 3, fig. 11 discloses a logic circuit 1109 with a first logic input and a second logic input, respectively coupled to the first and the second signals and adapted to detect the attainment of the respective prescribed state by the first and the second output signals, and in which said symmetrization means are associated with said first and second logic inputs.

As to claim 4, the symmetrization means 1113 and 1115 are seen as decoupling means of the first and second inputs (i.e., being enable) of the reset circuit from the first and second logic inputs, respectively.

As to claim 5, figure 2 discloses a phase difference detector 201 adapted to detect a phase difference between a reference signal (i.e., output of RERF. OSCF) and a signal derived from the output signal (Fout), and an oscillator 209 controlled by a phase difference signal (output of 201) generated by the phase difference detector, characterized in that the phase difference detector is realized according to claim 1 (See the rejection of claim 1 as noted above).

As to claims 6 and 7, figure 2 and its associated description disclose the frequency divider 205 being an N-fractional divider controlled by delta-sigma modulator 211. Therefore, its dividing factor is either an integer number or an average division factor equal to a non-integer number.

As to claim 21, col. 10, line 54, discloses bistable element being flip-flop devices.

As to claim 8, the scope of claim is similar to that of claim 5. Therefore, it is rejected for the same reason set forth above. Further, it is inherent that there exists a generator to generate a reference signal.

As to claim 22, col. 10, line 54, discloses bistable element being flip-flop devices.

As to claim 23, figure 11 discloses delay 1111 coupled to the symmetrization element for providing a delay to the first and second bistable elements.

As to claim 9, it is rejected for reciting a method/step derived from an apparatus of claim 1 which is rejected as noted above.

As to claim 15, the scope of claim is similar to that of claim 1. Therefore, it is rejected for the same reason set forth above. It is noted that NAND gate is seen as a feedback circuit and its output coupled to delay 1111 is seen as feedback line.

As to claim 11, fig.11 shows a delay circuit 1111 for providing a timed delay from the outputs to the control inputs of the first and second logic elements.

As to claim 12, fig.11 shows the control input terminal being a feedback terminal.

As to claims 16-19, the scopes of claims are similar to that of claims 15, 11 and 22. Therefore, they are rejected for the same reasons set forth above.

As to claim 20, figure 1 discloses a PLL circuit including a phase difference detector for realizing frequency synthesizer.

Response to Arguments

5. Applicant's arguments filed 2-15-06 have been fully considered but they are not persuasive.

Regarding the rejection of claims based on the Partovi reference, Applicant interprets incorrectly the rejection. The rejection of claims calls for a basic representation of inverter comprising two transistors connected in series, not each inverter comprising a single transistor.

Regarding the rejection of claims based on the Nilsson and Pricier references, Applicant has argue that "*the transistors 34 and 35 of Pricier are clearly coupled in parallel (via the nodes 42 and 36)*" is not persuasive since transistors 34 and 35 are in series connection (i.e., same branch) between the high power potential 33 and the low potential 37. Transistors 34 and 35 are neither in series connection nor in parallel connection with respect to nodes 36 and 42 since there is no current nor voltage passing between nodes 36 and 42.

Conclusion

6. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

7. Any inquiry concerning this communication or earlier communications from the examiner should be directed to An T. Luu whose telephone number is 571-272-1746. The examiner can normally be reached on 7:30-5:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Timothy P. Callahan can be reached on 571-272-1740. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

An T. Luu
3-20-06

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